REMARKS

The following remarks are submitted as a full and complete response to the outstanding Action. By this Amendment, claims 1, 8-13 and 15-17 have been amended to more particularly set forth the application. No new matter has been introduced. Claims 1-17 are currently pending and therefore submitted for consideration.

Section 102 Rejection

Claims 12-15 and 17 have been rejected under 35 U.S.C. §102(e) as being anticipated by Knox, et al. (of record, hereinafter *"Knox"*).

The basis and reference cited for this rejection are identical to those set forth in the previous Office Action dated December 19, 2002. Additionally, it is asserted in item 1 of outstanding Action that the distinguishing features argued in the previous filed Amendment dated March 14, 2003, are not set forth in the claims.

Claim 12 from which claims 13-15 depend and claim 17 have been amended to particularly set forth that the additional data are written in with the additional area's address. It is respectfully submitted that ***Knox*** does not disclose or teach such added limitation as now set forth in claims 12-15 and 17.

In other words, ***Knox*** does not disclose or teach that data are written in with the address of an additional data taken into account, and is particularly silent with respect to writing bitstreams. Instead, ***Knox*** merely discloses the generation of digital words representative of luminance and chrominance signals (see e.g., 4: 32-37).

Additionally, with respect to claims 12 and 17, the Examiner purported that in connection with setting the storage circuit, ***Knox*** teaches that a plurality of data are stored in the memory 140, including image data and an OSD bit map as data other than image data, and the region of OSD bit map is defined as an additional area. ***Knox*** discloses that (1) the ODS unit restores the OSD bitstreams from the storage unit, (2) the OSD bitstreams include an OSD header and OSD data, and (3) the decoding system 100 includes a processor 130 having an input supplied with bitstreams 110 and 120. ***Knox*** also discloses that bitstreams 120 are real time audio and video compressed data, and bitstreams 110 are control signals or data not included in the bitstreams 120. Particularly, in column 2, lines 65-66 of ***Knox***, it is disclosed that the bitstreams 120 received by the processor 130 are stored in the memory 140 through the video decoder 160.

However, ***Knox*** fails to explicitly disclose that the bitstreams 110 are stored as actual data. ***Knox*** is also silent regarding the step of storing data other than image data. Although ***Knox*** refers to the step of supplying and storing bitstreams 120 (image data) in the memory 140 from the processor 130 (see 4: 30-35), it is silent with respect to reading out image data and data other than image data from the storage circuit.

As to claim 13, ***Knox*** does not disclose that data read out from the storage circuit but the processor 130 supplied with the bitstreams 120 and 110 (see 2: 48-55).

As per claim 14, ***Knox*** merely teaches that the processor 130 supplies, e.g. the video decoder 160 and OSD unit 150 with control data, and not the first write control

signal supplied to the storage circuit and the transfer enable signal enabling an execution of processing as set forth in claim 14 (see 2: 48-64).

Still further with respect of claim 15, ***Knox*** teaches that the video decoder 160 and OSD unit form streams or sequences of digital words representing luminance and chrominance components, and the sequences of video components are mixed via the mixer 170 (see 4: 30-37). However, ***Knox*** does not teach that the insertion of data from the additional area into a predetermined position of a video signal.

Accordingly, it is respectfully submitted that claims 12-15 and 17 are allowable over ***Knox***.

Section 103 Rejections

Claims 1-2, 11 and 16 are rejected under 35 U.S.C. §103(a) as being unpatentable over *Sherburne* (of record) in view of *Knierim* (of record).

Claims 1 and 16 have been amended to particularly set forth that the additional data are written in with the additional area's address. Accordingly, claim 1 from which claims 2 and 11 depend and claim 16 are allowable over ***Sherburne*** and ***Knierim***. That is, neither ***Sherburne***,nor ***Knierim*** teaches or suggests the added limitation as now set forth in claims 1, 2 ,11 and 16.

Additionally, the last paragraph of claim 1 specifically requires that the image data adjust the address generated by the address generation circuit. Such "adjustment" refers to data written in with the address of the additional area taken into account.

Still further, ***Sherburne*** teaches that address locations contain image data with the preceding or following address location containing the associated overlay data (see 2: 29-45). However, as illustrated in Figs. 4, 5A and 5B, ***Sherburne*** merely teaches carrying out fixedly the bit conversion from input to output, which differs from the area adjustment circuit of the present application, which is adapted to write data having a width adjusted with an additional area taken into account.

More specifically with respect to claims 1 and 6, the Examiner purported that the memory 30 of ***Sherburne*** corresponds to the storage circuit as set forth in the present application. The Examiner also referred to the disclosure in ***Sherburne*** regarding "the general organization of the memory and memory data, and the circuit for reading out and utilizing the same" (see item 2, page 2 of the outstanding Action) as teaching the data input/output circuit and the access control circuit recited in claim 1.

Moreover, the Examiner purported that the disclosure in ***Sherburne*** with respect to addressing a memory plane associated with an image frame would suggest the address generation circuit as set forth in the present application, and that the interleaving of the overlay data with the image data in ***Sherburne*** would suggest the area adjustment circuit as set forth in the present application. The Examiner concluded that the refresh circuit not disclosed in ***Sherburne*** is taught by ***Knierim***, and thus purportedly rendering claim 1 obvious over ***Sherburne*** in view of ***Knierim***.

However, the disclosure in ***Sherburne*** regarding the access control circuit and the area adjustment circuit may only be pertinent to the general memory circuit and reading data out from the memory. Indeed, the presence of these circuits in ***Sherburne***

does not provide adequate support for the implied relationship between the circuits. Particularly, the ground for the area adjustment circuit is presumed and not logically supported.

By contrast, claim 1 requires that the access control circuit controls access of writing in and reading out the image data to and from the storage circuit, and that the area adjustment circuit adjusts the address generated by the address generation circuit so as to store additional data other than the image data in an additional area. Moreover, in claims 16 and 17, the adjustment is defined as in address space for image data which is of a width same as an address space for additional data other than image data. It is noted that the additional area in ***Sherburne*** set forth preceding or following an area for image data is merely a result from writing data interleavingly. Such is completely different from the address set for an additional area as recited in claim 2.

Claims 1-2, 11 and 16 are therefore neither taught nor suggested by ***Sherburne*** and ***Knierim***, individually or in combination.

Claims 3, 5-7 and 8-10 are rejected under 35 U.S.C. §103(a) as being unpatentable over *Sherburne* in view of *Knierim* and further in view of *Knox*.

Claim 1 has been amended to particularly set forth that the additional data are written in with the additional area's address. Accordingly, claims 3, 5-7 and 8-10, which depend directly or indirectly from claim 1, are patentable over ***Sherburne***, ***Knierim*** and ***Knox*** for at least the reasons stated above with respect to claim 1. That is,

Sherburne, ***Knierim*** and ***Knox***, individually or in combination, fail to teach or suggest the added limitation as now set forth in claims 3, 5-7 and 8-10.

Claim 4 is rejected under 35 U.S.C. §103(a) as being unpatentable over *Sherburne* in view of *Knierim* and further in view of Herz, et al. (of record, hereinafter *"Herz"*).

Claim 4 is also patentable over ***Sherburne*** and ***Knierim*** for at least the reasons stated above with respect to claim 1 from which claim 4 depends. Additionally, ***Herz*** does not supplement for the deficiency of ***Sherburne*** and ***Knierim*** with respect to the newly added limitation and therefore claim 4 is allowable over ***Herz*** as well.

Additionally, the Examiner relied on ***Herz*** for teaching that the closed caption text data are transmitted during the vertical blanking interval (VBI). However, nothing is taught in ***Herz*** regarding the area adjustment circuit using such information to set the size of an additional area as required by claim 4. It is therefore respectfully submitted that claim 4 is neither taught nor suggested by ***Sherburne*** in view of ***Knierim*** and ***Herz***.

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In view of the foregoing, reconsideration of the application, withdrawal of the outstanding rejections, allowance of claims 1-17, and the prompt issuance of a Notice of Allowability are respectfully solicited.

If this application is not in condition for allowance, the Examiner is requested to contact the undersigned at the telephone listed below.

The Commissioner is hereby authorized to charge any fee deficiency or credit any overpayment associated with this communication to Deposit Account No. 01-2300.

Respectfully submitted,

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